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| **ASSIGNMENT** | |
| **Course Code** | 19CSC204A |
| **Course Name** | Logic Design |
| **Programme** | B. Tech |
| **Department** | Computer Science & Engineering |
| **Faculty** | Faculty of Engineering Technology |

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| **Reg. No** | 18ETCS002121 |
| **Semester/Year** | 3RD / 2019 |
| **Course Leader/s** | Mr. Narasimha Murthy K. R. and Mr. V. Deepak |

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| **Declaration Sheet** | | | | | | | | |
| Student Name | SUBHENDU MAJI | | | | | | | |
| Reg. No | 18ETCS002121 | | | | | | | |
| Programme | B. Tech | | | | | Semester/Year | 3rd / 2019 | |
| Course Code | 19CSC204A | | | | | | | |
| Course Title | Logic Design | | | | | | | |
| Course Date |  | | To | |  | | | |
| Course Leader | Mr. Narasimha Murthy K. R. and Mr. V. Deepak | | | | | | | |
| **Declaration**  The assignment submitted herewith is a result of my own investigations and that I have conformed to the guidelines against plagiarism as laid out in the Student Han  dbook. All sections of the text and results, which have been obtained from other sources, are fully referenced. I understand that cheating and plagiarism constitute a breach of University regulations and will be dealt with accordingly. | | | | | | | | |
| Signature of the Student | |  | | | | | Date |  |
| Submission date stamp  (by Examination & Assessment Section) | |  | | | | | | |
| Signature of the Course Leader and date | | | | Signature of the Reviewer and date | | | | |
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| **Faculty of Engineering and Technology** | | | |
| Ramaiah University of Applied Sciences | | | |
| Department | Computer Science and Engineering | Programme | B. Tech. in CSE |
| Semester/Batch | 3rd Semester/2018 | | |
| Course Code | 19CSC204A | Course Title | Logic Design |
| Course Leaders | Mr. Narasimha Murthy K. R. and Mr. V. Deepak | | |

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|  | | | | | |
| Sections | Marking Scheme | | Marks | | |
| Max Marks | First Examiner Marks | Moderator |
| Question 1 |  | | | | |
| **A** | **Introduction** | **01** |  |  |
| **B** | **Circuit Design** | **04** |  |  |
| **C** | **Simulation of Circuit** | **03** |  |  |
| **D** | **Circuit using NAND Gates** | **02** |  |  |
|  | **Question 1 Max Marks** | **10** |  |  |
| Question 2 |  | | | | |
| **A** | **Introduction** | **01** |  |  |
| **B** | **Circuit Design** | **03** |  |  |
| **C** | **Simulation of Circuit** | **02** |  |  |
| **D** | **Circuit using Ex-OR Gates** | **04** |  |  |
|  | **Question 2 Max Marks** | **10** |  |  |

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| **Course Marks Tabulation** | | | | |
| **Component-1 (C) Assignment** | **First Examiner** | **Remarks** | **Moderator** | **Remarks** |
| **Question 1** |  |  |  |  |
| **Question 2** |  |  |  |  |
| **Marks (out of 20 )** |  |  |  |  |
| **Signature of First Examiner Signature of Moderator** | | | | |

# **Question No. 1**

**Solution to Question No. 1:**

## Introduction to the functionality of the circuit

A calculator is a device that performs arithmetic operations on numbers. The simplest calculators can do only addition, subtraction, multiplication, and division.

We are taking two 2-bit binary number as input. And getting 4-bit binary numbers output.

From fig 1:



And 2-bit selector lines choose which operations to perform.

|  |  |  |
| --- | --- | --- |
| Selector lines | | operation |
| S1 | **S0** |
| 0 | **0** | addition |
| 0 | **1** | subtraction |
| 1 | **0** | multiplication |
| 1 | **1** | division |

Fig 1 shows block diagram of adder, subtractor, multiplier and divider circuit.

|  |  |  |  |
| --- | --- | --- | --- |
| Figure Number | Circuit Name | Inputs | Outputs |
| 2 | Adder | **A1, A0 --- B1, B0** | **S3, S2, S1, S0** |
| 3 | Subtractor | **A1, A0 --- B1, B0** | **D3, D2, D1, D0** |
| 4 | Multiplier | **A1, A0 --- B1, B0** | **P3, P2, P1, P0** |
| 5 | Divider | **A1, A0 --- B1, B0** | **Q1, Q0 --- R1, R0** |

## Circuit design using Logisim

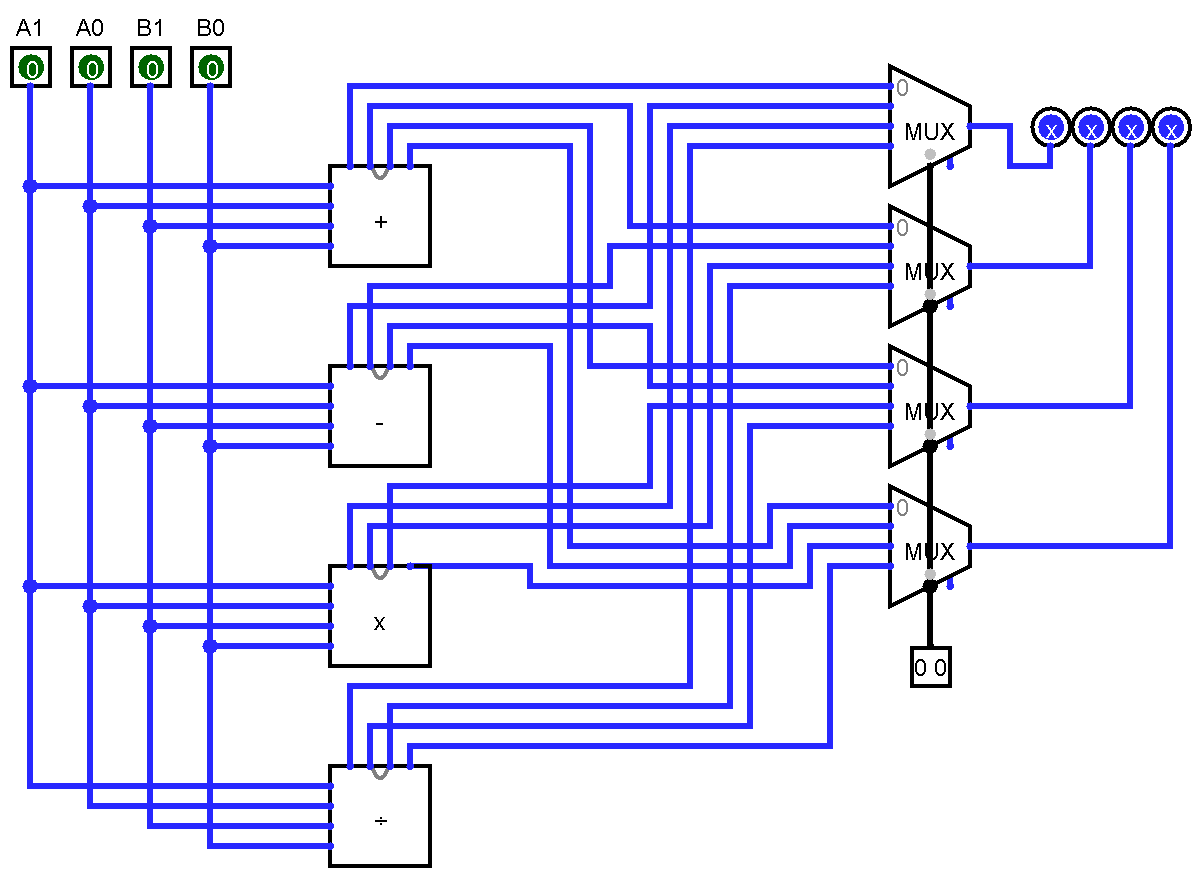


Figure combined circuit for all the operations

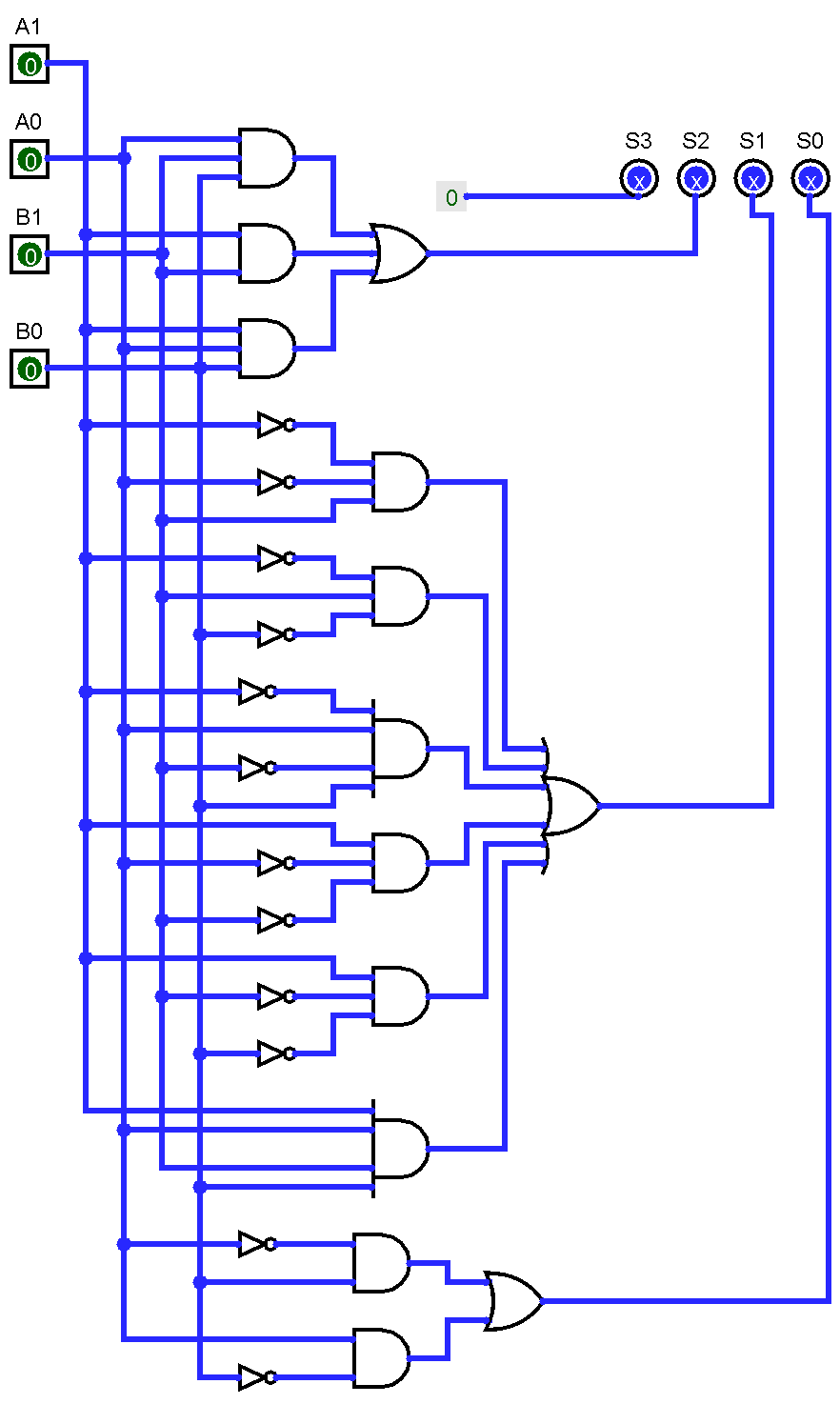


Figure adder circuit using basic gates

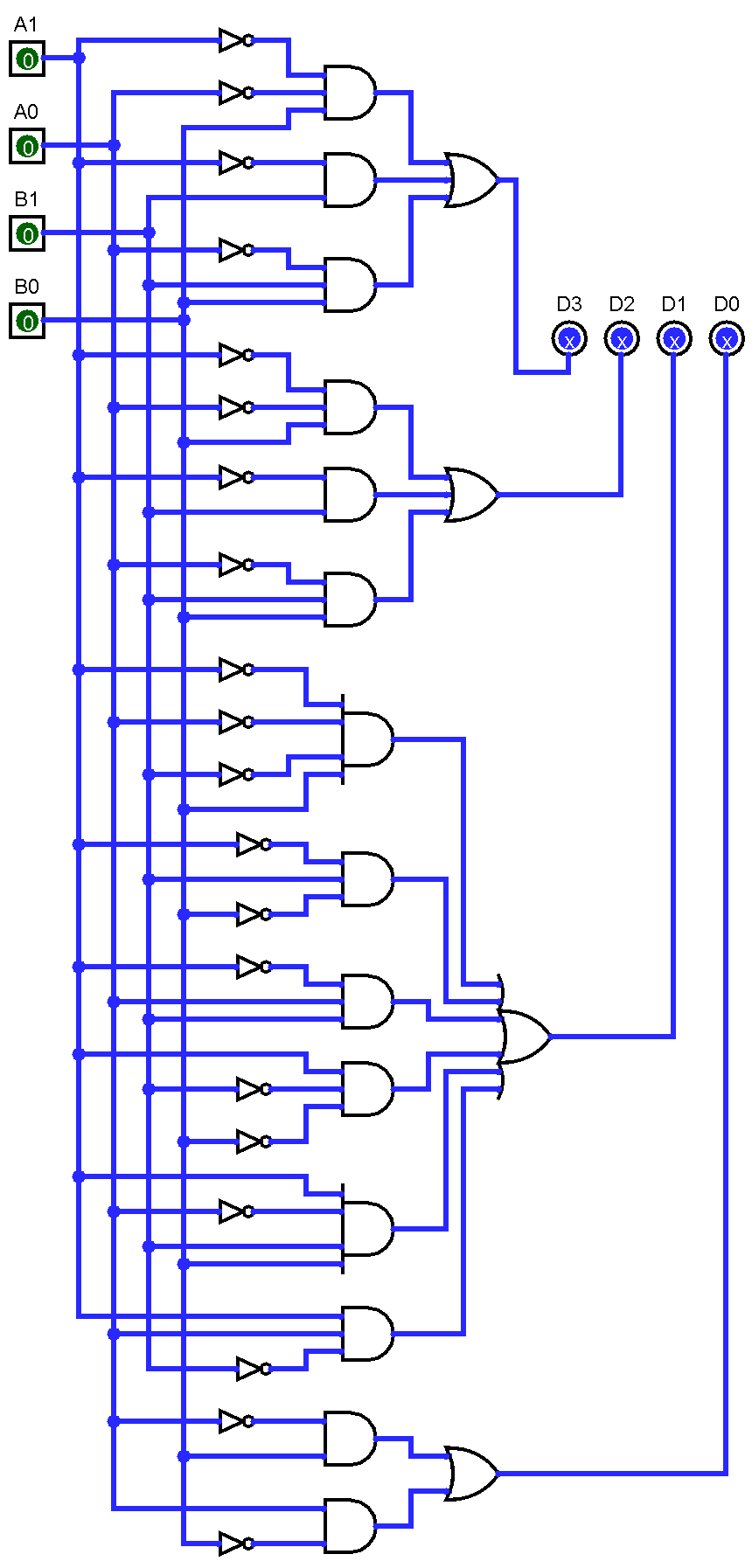


Figure subtraactor using basic gates

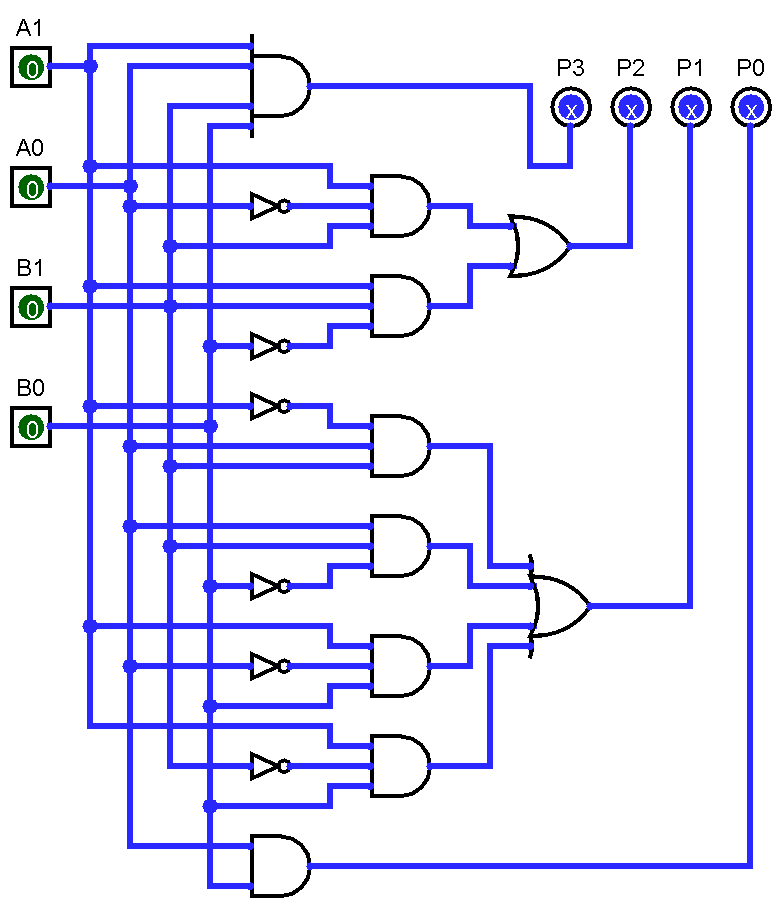


Figure multiplier using basic gates

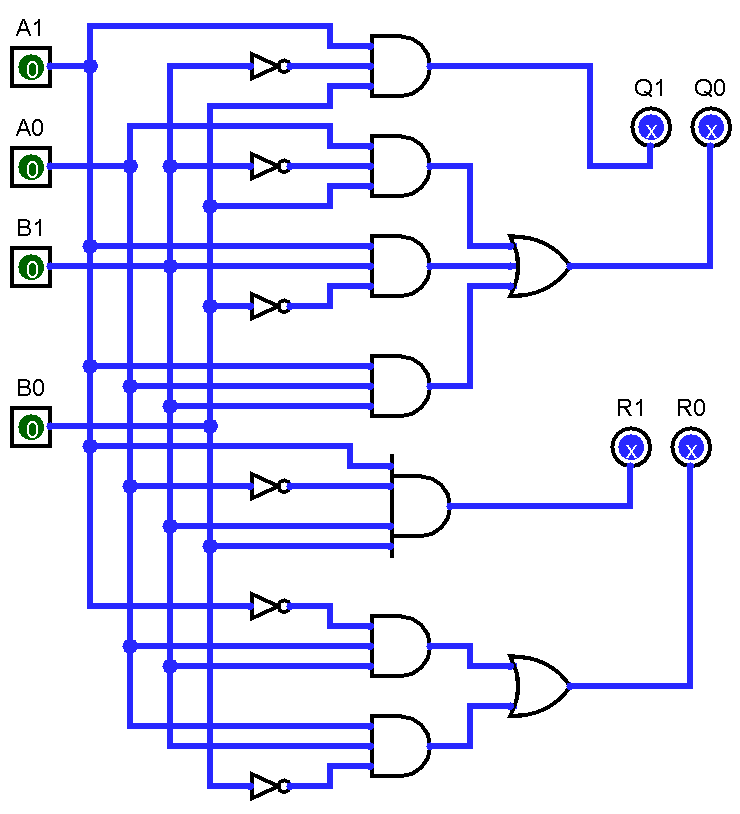


Figure divider using basic gates

## Simulation of the designed circuit

Adding and , which is giving output **.**

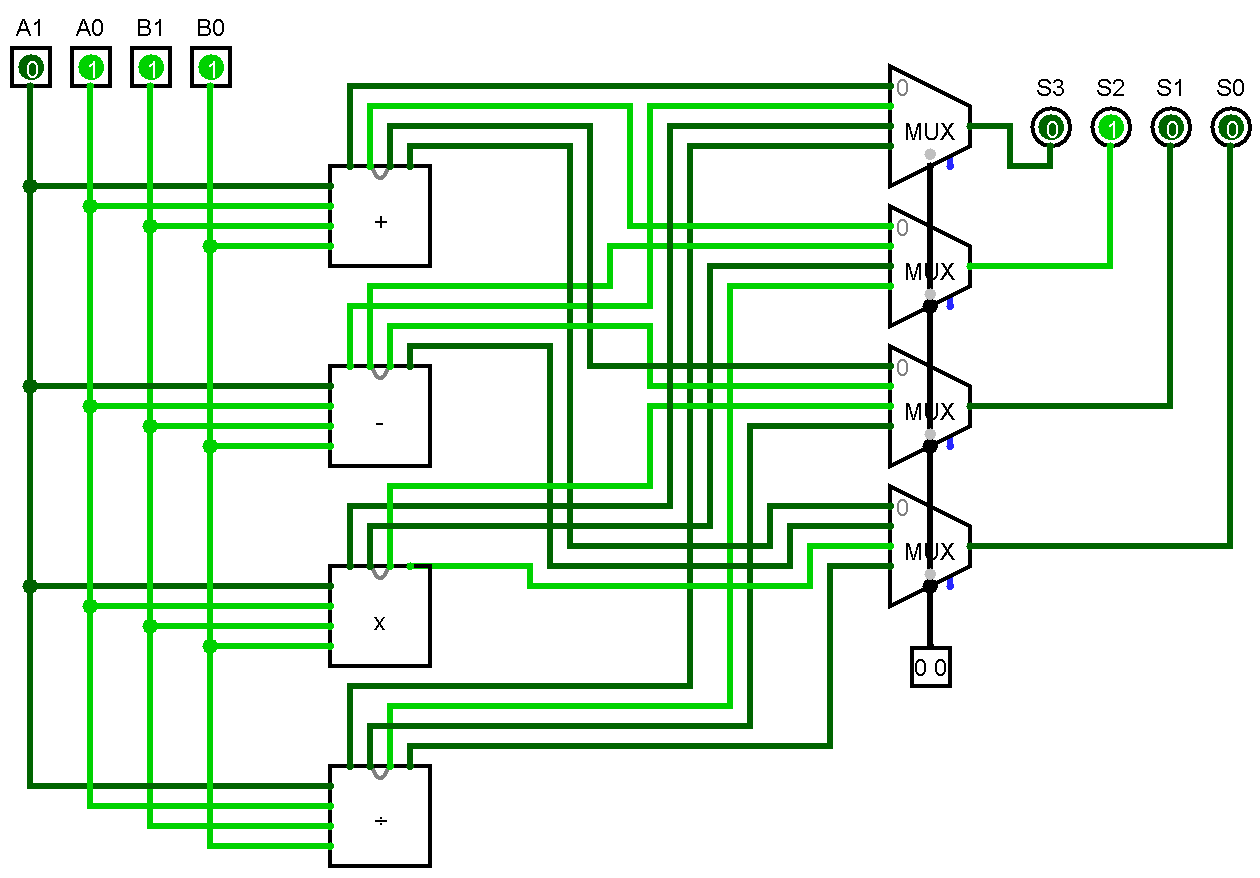


Figure simulation of adder (adding 1 and 3 )

Subtracting and , which is giving output **.**

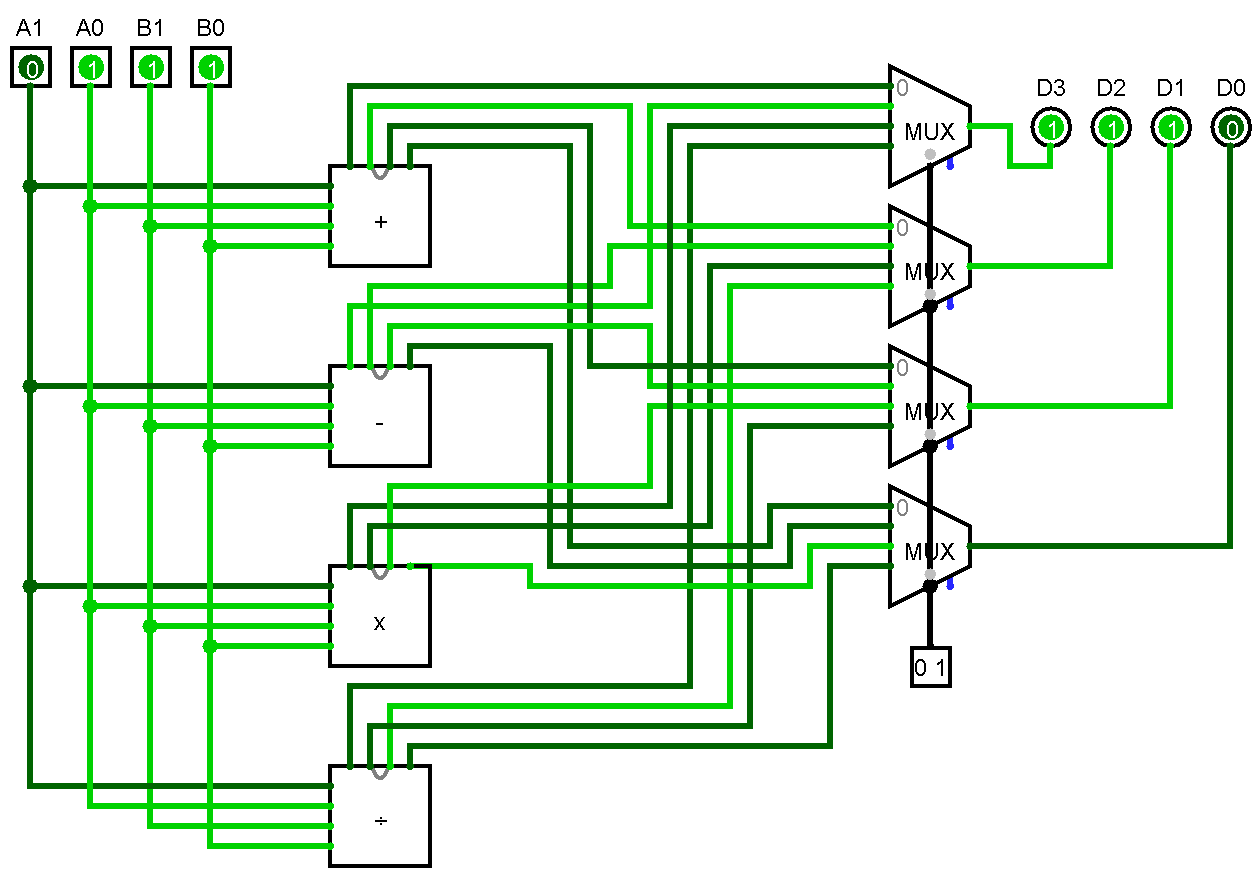


Figure simulation of subtractor (subtracting 1 and 3 )

Multiplying and , which is giving output **.**

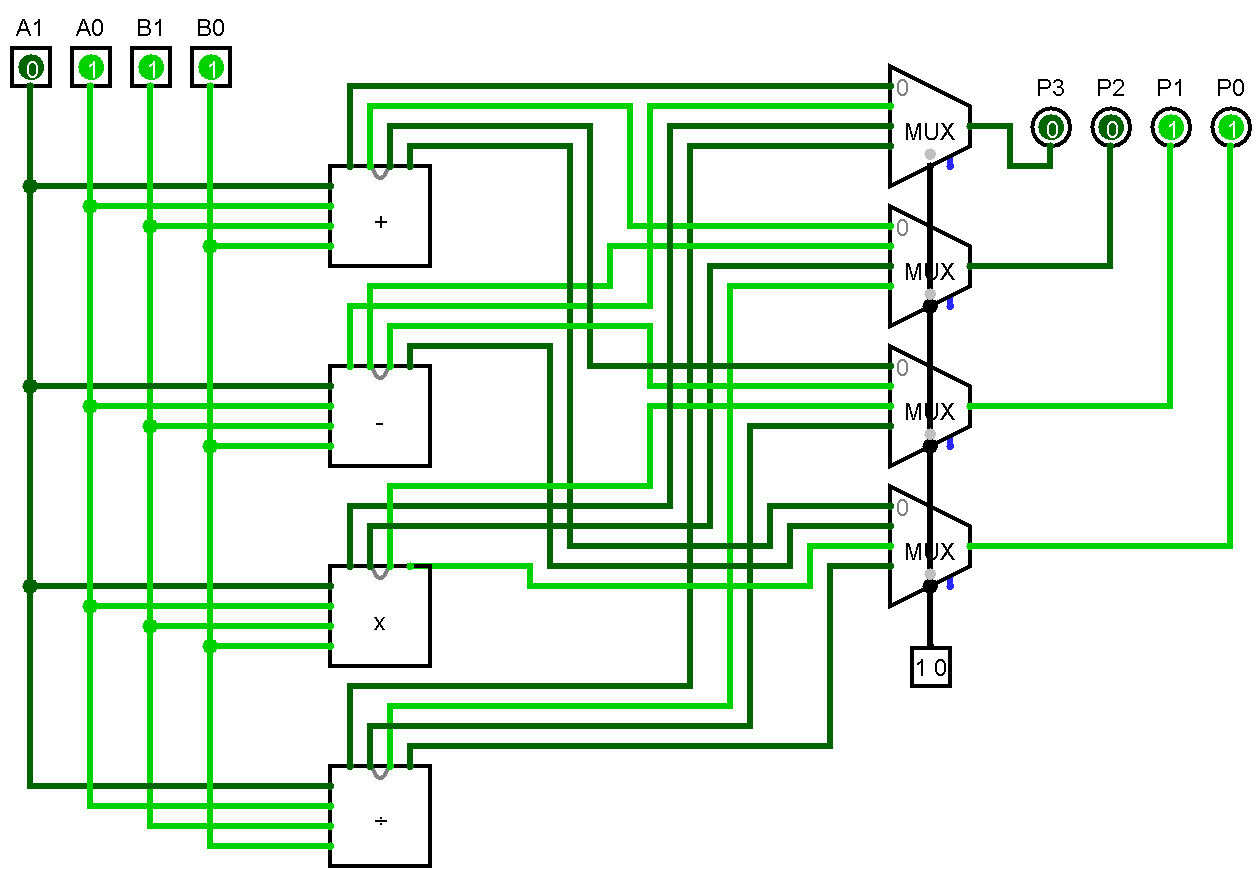


Figure simulation of multiplying (multiplying 1 and 3 )

Dividing and , which is giving output **.**

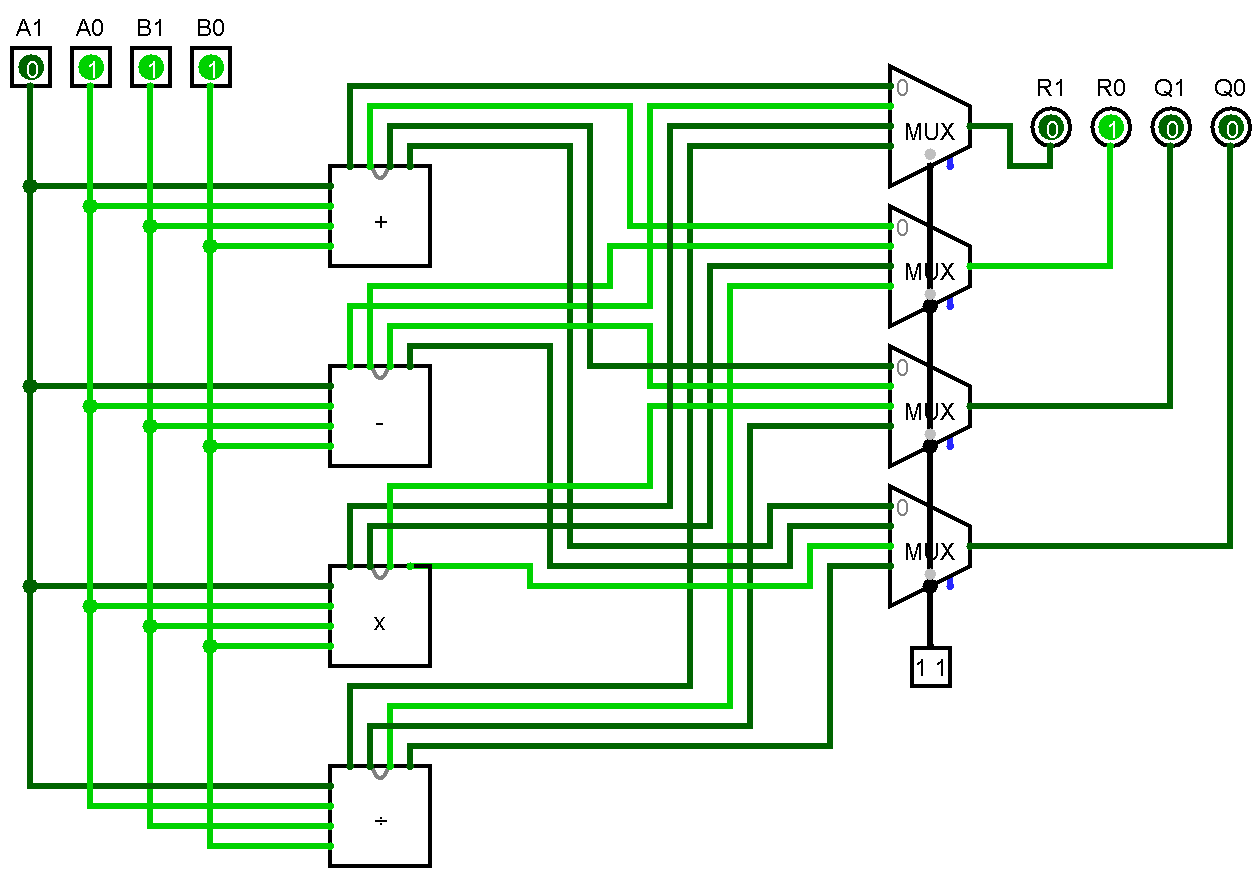


Figure simulation of divider (dividing 1 and 3 )

## 1.4 Changes in the circuit if you had to implement it using only NAND gates

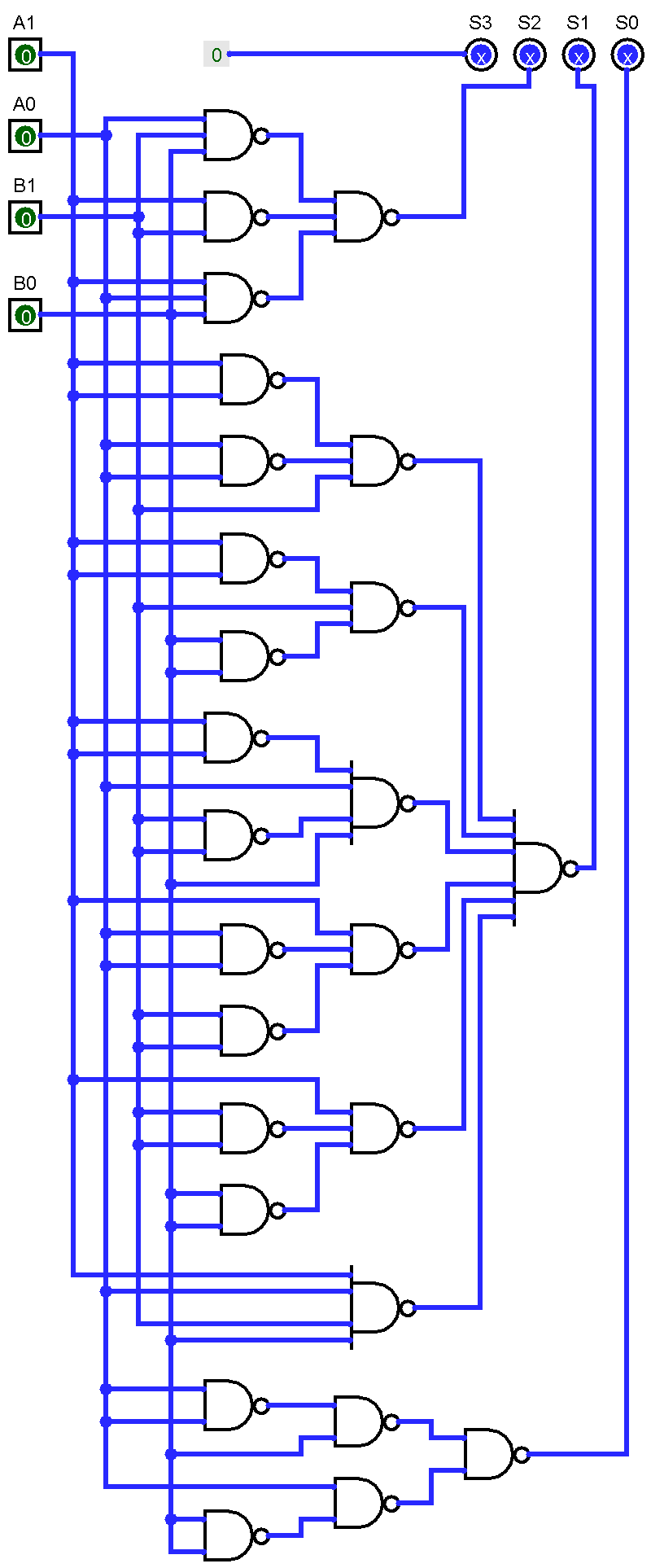


Figure adder circuit using NAND gates

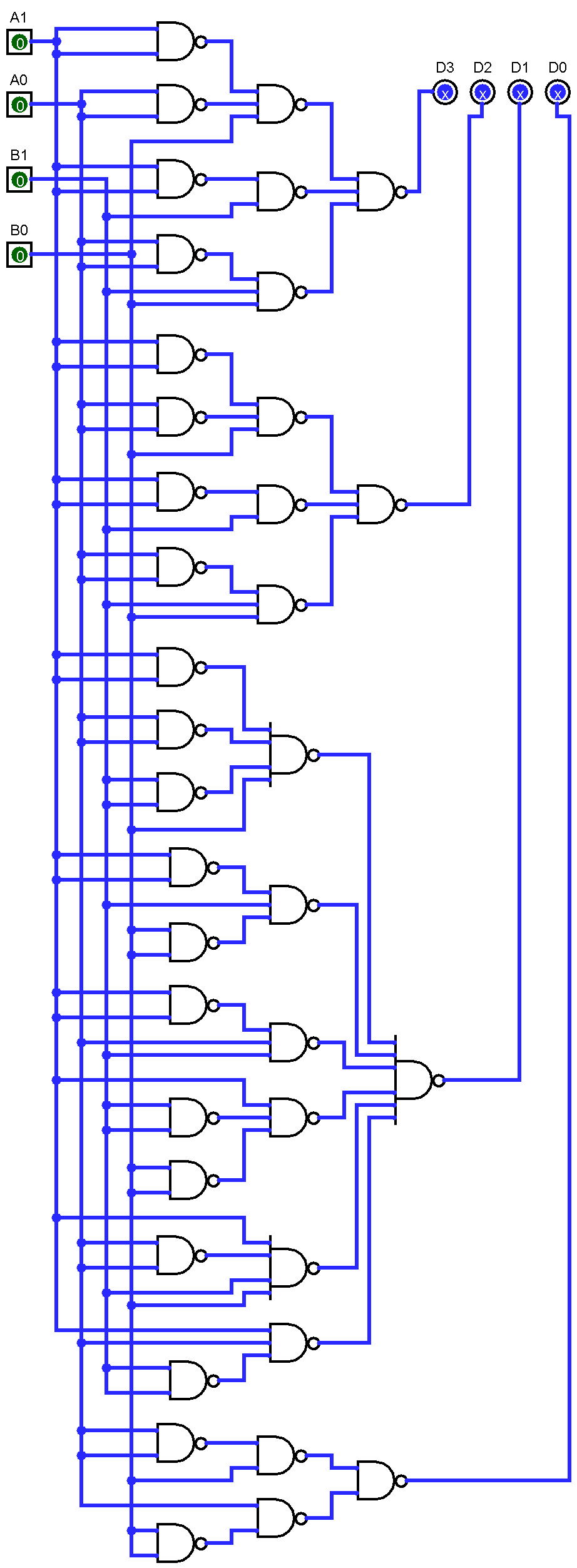


Figure subtractor circuit using NAND gates

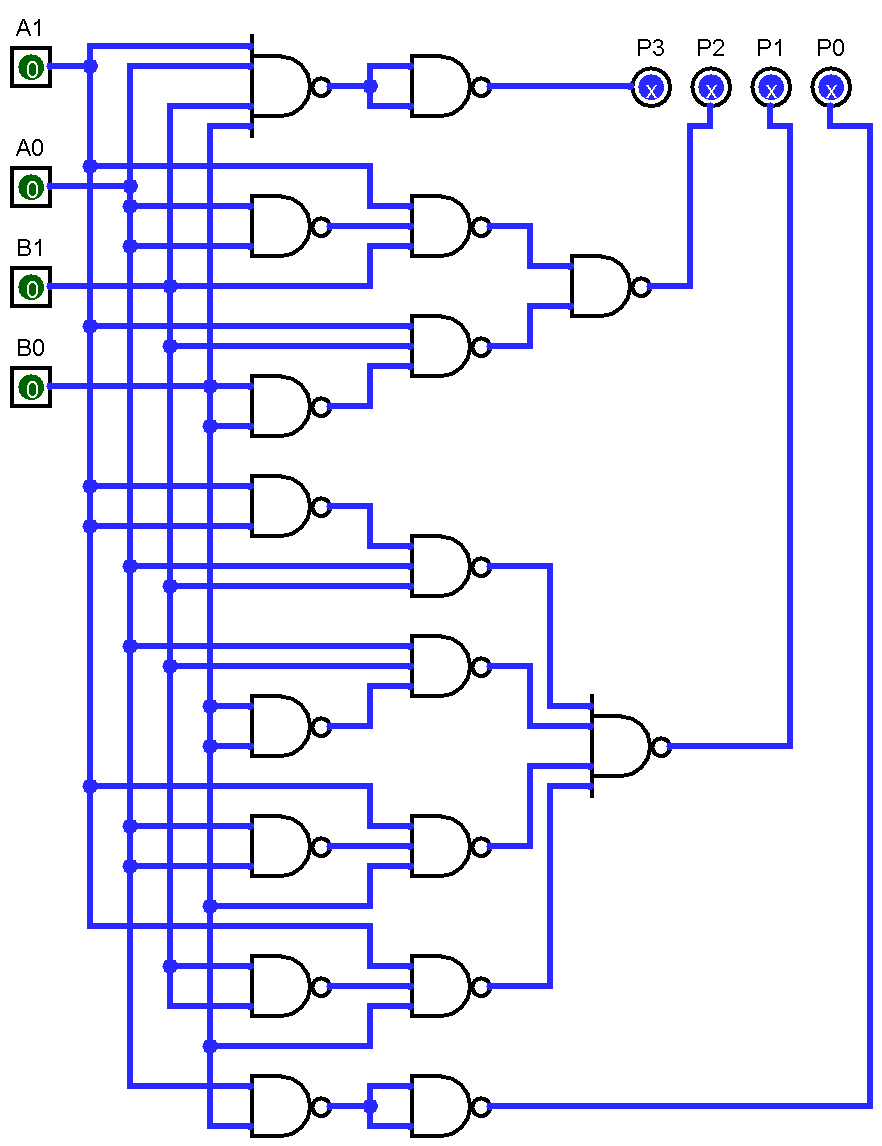


Figure multiplier circuit using NAND gates

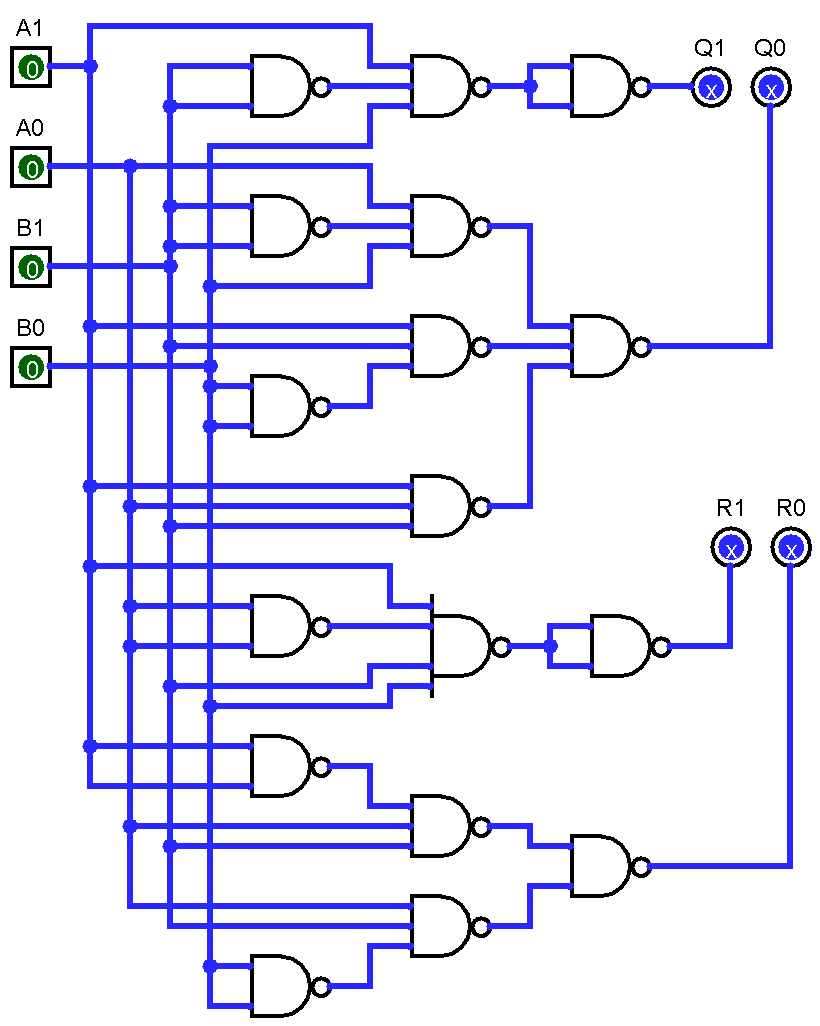


Figure divider circuit using NAND gates

# **Question No. 2**

**Solution to Question No. 2:**

## 2.1 Introduction to the functionality of the circuit

## This is a combinational circuit that generates 2’s complement of a 4-bit input binary number.

It takes as input and gives ) which is 2’s complement of A as output.

Equations:

## 2.2 Circuit design using Logisim

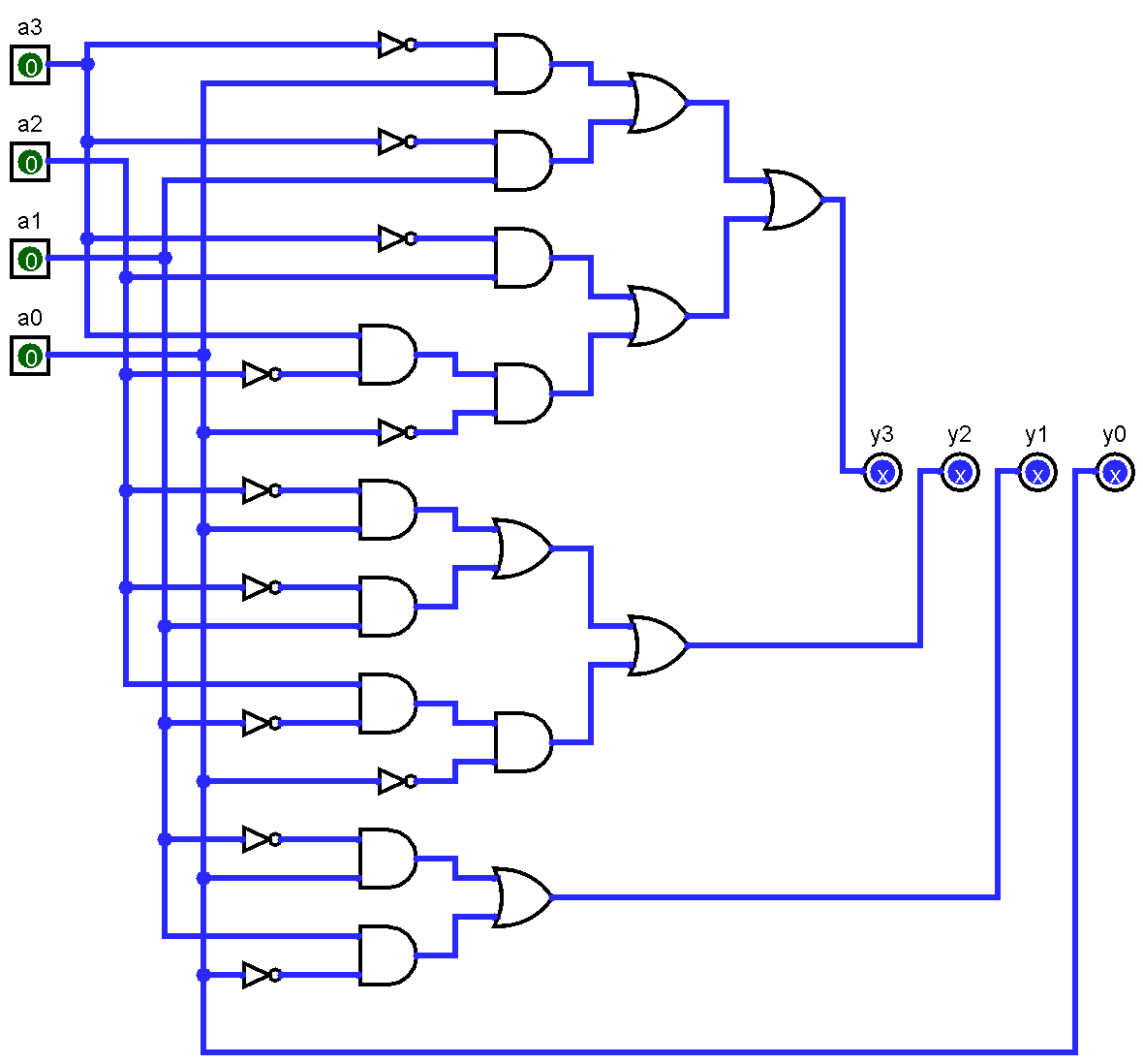


Figure 2’s complement calculator using basic gates

## 2.3 Simulation of the designed circuit

In Fig 15,

We can see for we are getting , which is the 2’s complement of A.

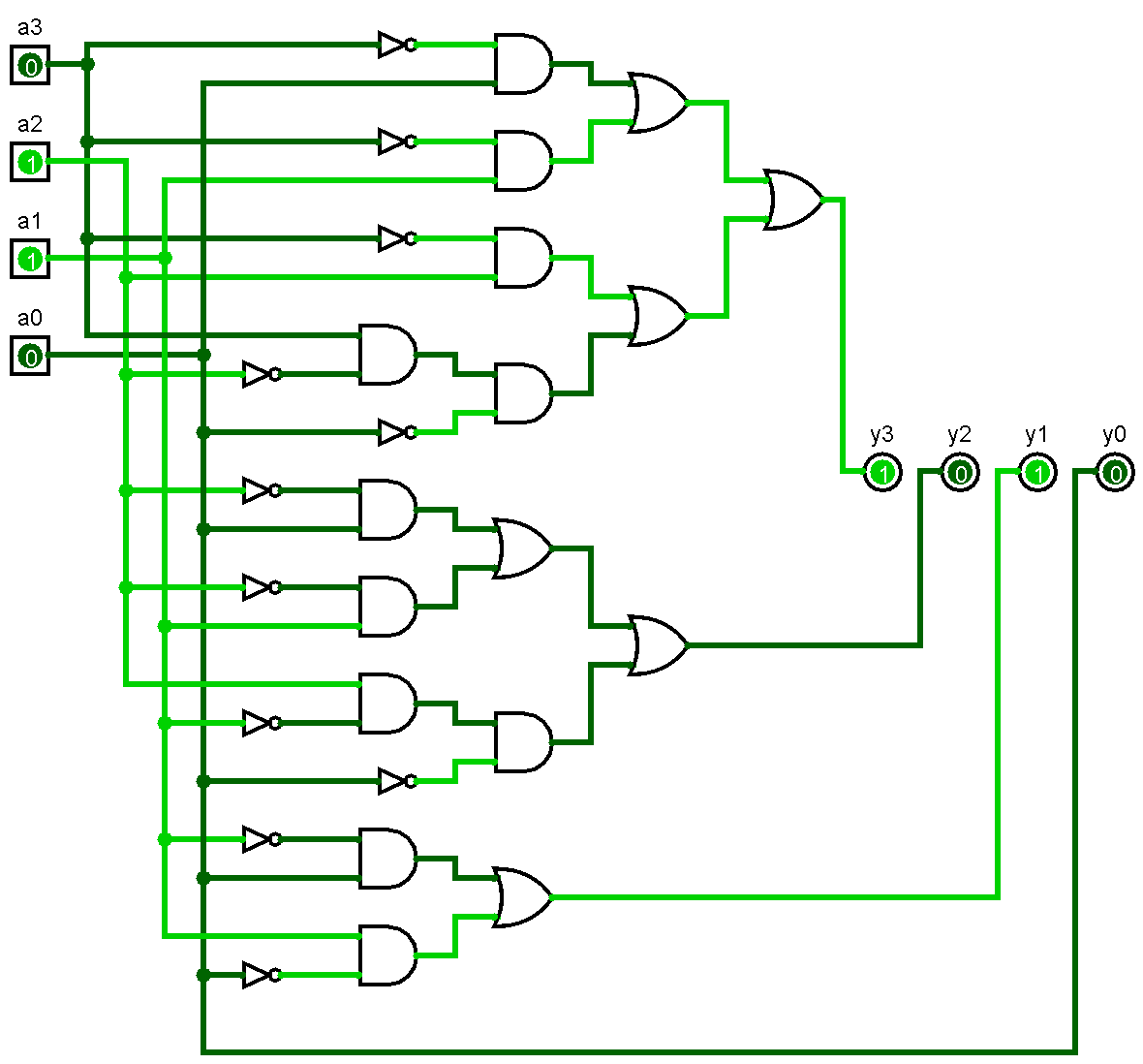


Figure simulating 2’s complement calculator

## 2.4 Changes in the circuit if you had to implement it using only XOR gates

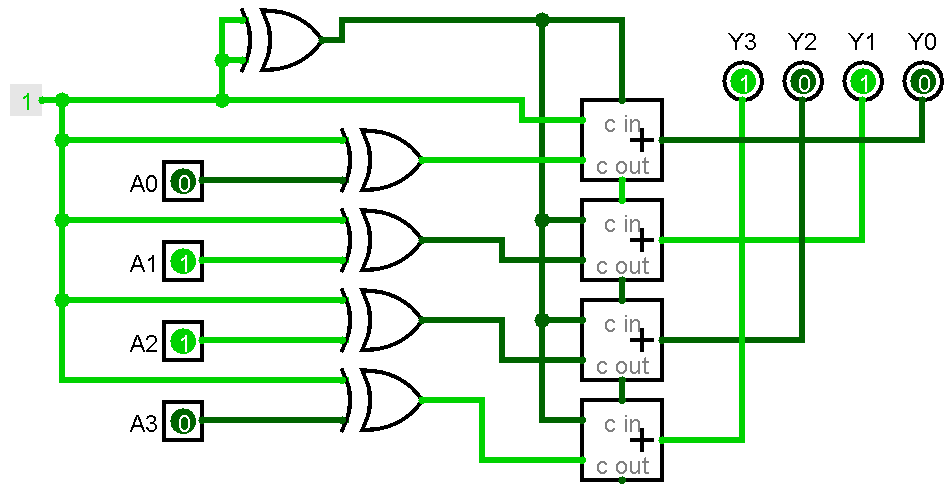


Figure 2’s complement calculator using XOR gate only.

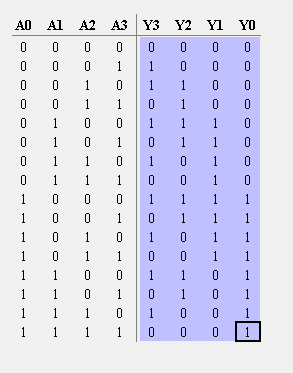


Figure truth table of 2's complement

# Bibliography

* Class notes / ppts
* <https://circuit-diagramz.com/circuit-diagram-calculator-using-logic-gates/>
* <https://rosettacode.org/wiki/Four_bit_adder>
* For Logisim files,
* Refer to: <https://github.com/subhendu17620/RUAS-sem-03/tree/master/LD%20lab/assignment/logisim%20files>